Managing Electrical Reliability During Layout Implementation

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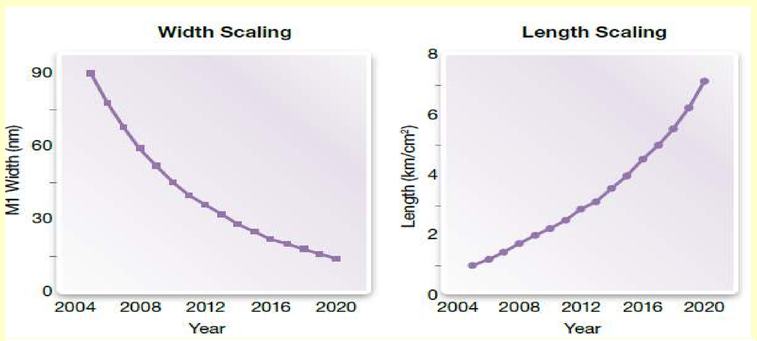
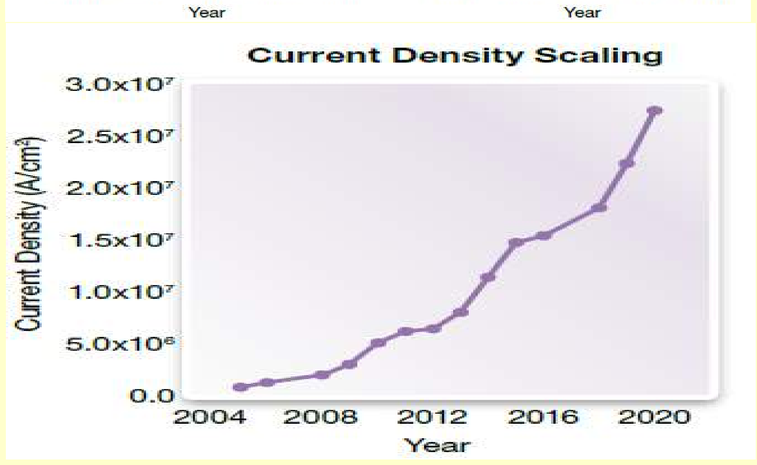
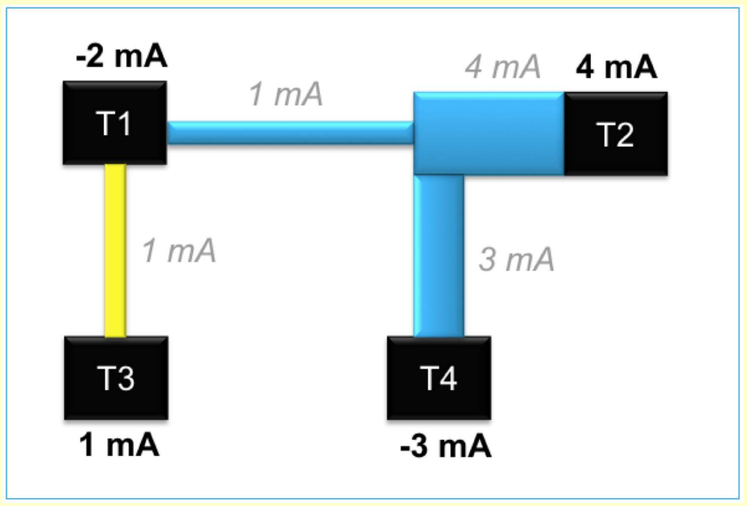
MOTIVATION

- **Tight Failure Rate Specification : 1ppm for Automotive and Industrial Application**
- **Power Hungry IP and SOC : Demand of high speed application products in lower technology nodes is leading to increase in current density.**
- **Technology : Graphs show the impact on metal dimensions and current density with technology shrinkage.**
- **Cost : Reducing Metal Mask, to make product more competitive**

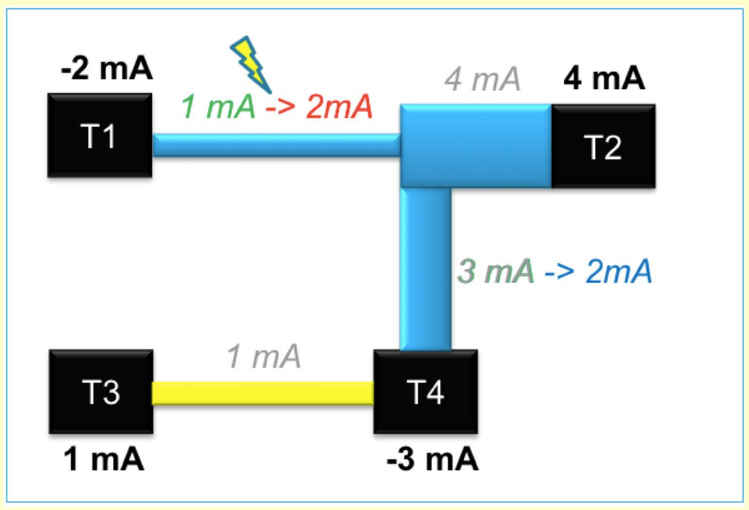




- **Need of knowing current topology during layout phase to avoid EM-IR and design iterations**

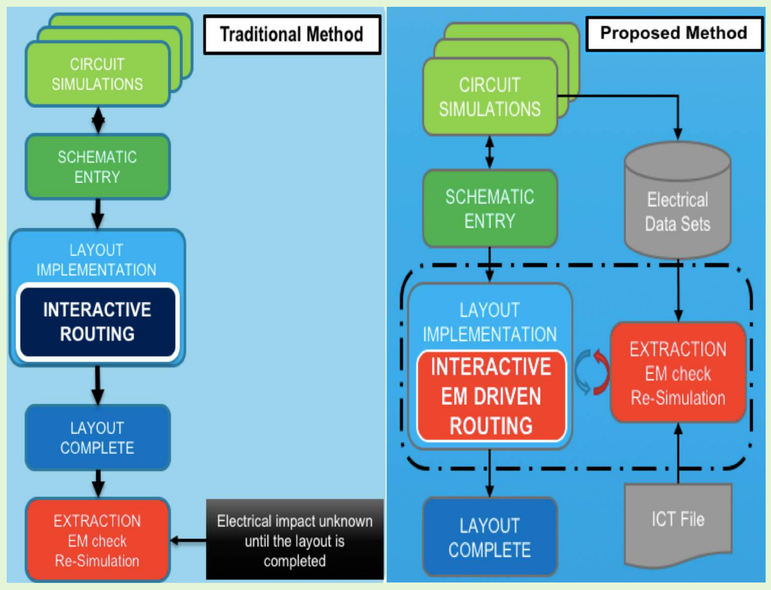


- **We need the final topology to be able to estimate the current going through all wires**

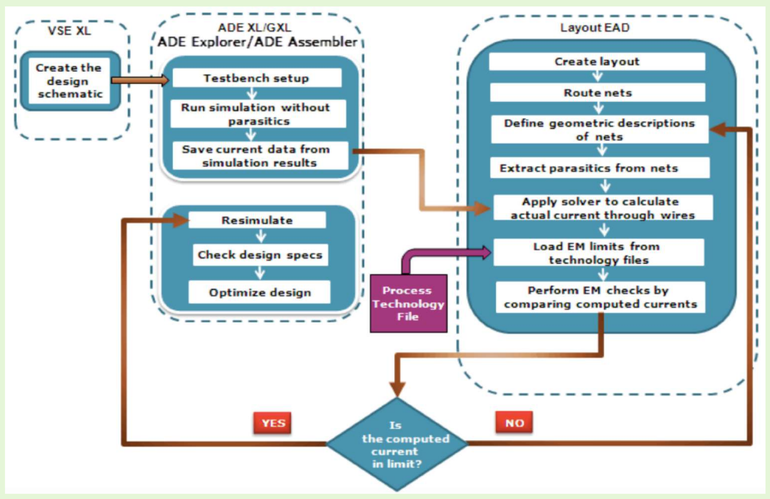


The proposed flow assists the user to achieve what he wants, while taking into account current density information

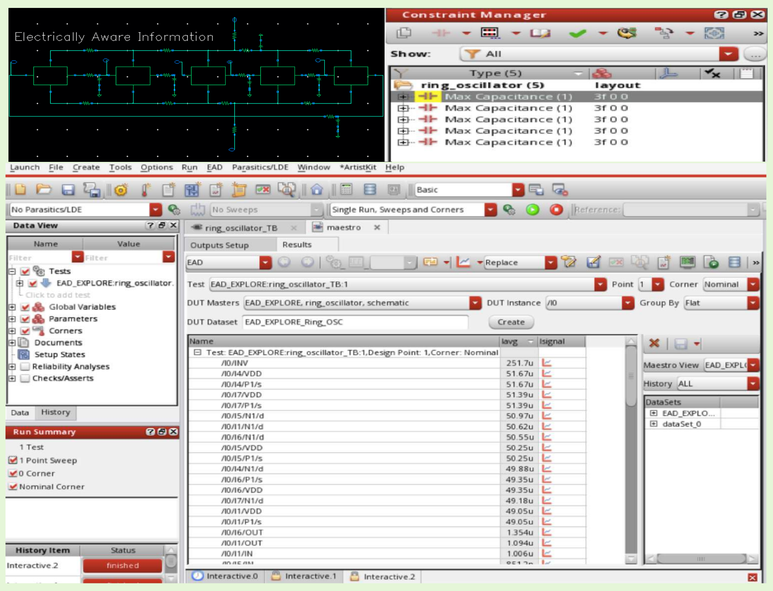
METHODOLOGY



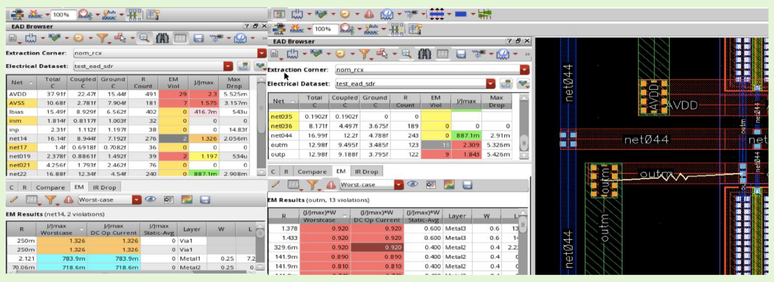
- **Post Edit Parasitics (RC) and EM/IR check, allows designer to check parasitics immediately after route is finished, using Virtuoso EAD without waiting till LVS or signoff**
- **During interactive routing step of the layout implementation the electromigration constraints are taken into account. It decreases the number of iterations.**
- **Simulation current driven interactive routing, allows designer to draw a net wire interactively with the width required to meet EM for peak current, using Virtuoso SDR**
- **Early EM optimize design and verify the performance and reliability**
- **Reducing signoff time and design iterations**



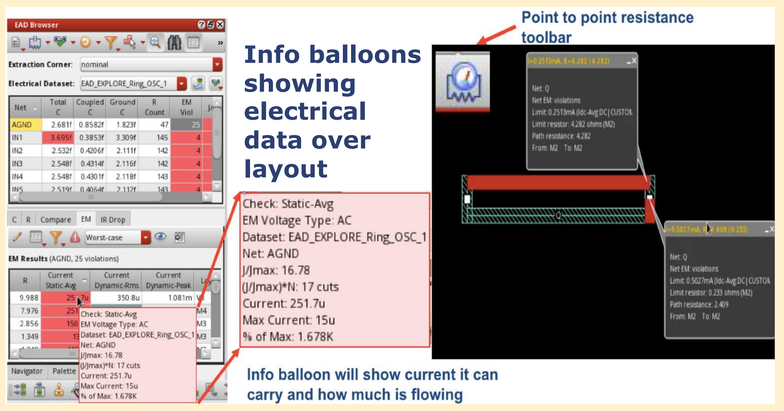
Setting electrical constraints and creating Current Dataset



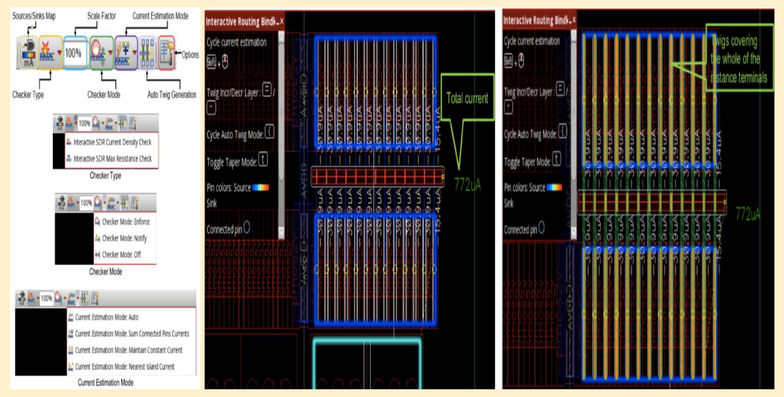
EAD Browser for Navigating & Analysing Parasitics and EM/IR Violations



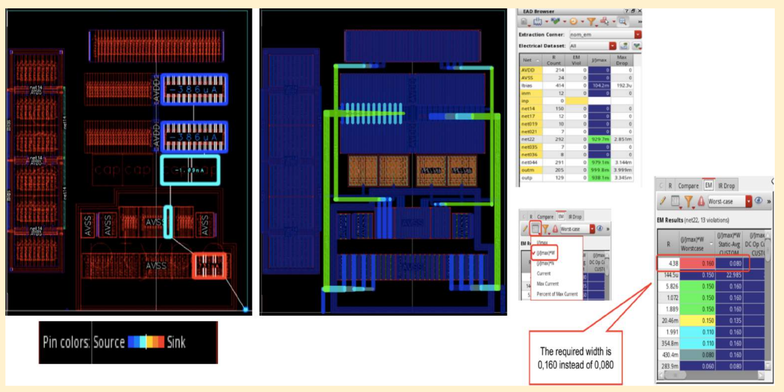
RESULTS



Simulation Driven Interactive Routing (SDR)



- **Guidance of current flow and it's distribution map w.r.t. total current, shown on layout while interactive routing**
- **Automatic sizing of wire and vias**
- **Automatic connection of twigs with metal and vias, meeting EM/current density constraints**



Real Time Parasitics w.r.t. signoff

Net Name	Sign-off C Extraction	EAD C Extraction	Accuracy
IN1	0.571f	0.556f	3%
IN2	0.574f	0.556f	3%
IN3	0.477f	0.441f	8%

*** capacitance results are fast and very close to signoff, which minimizes iterations and gap between schematic and post layout simulation**

Net Name	Sign-off R Extraction	EAD R Extraction	Accuracy
IN1	9.17 Ohm	9.56 Ohm	5%
IN2	9.16 Ohm	9.54 Ohm	5%
IN3	9.19 Ohm	9.56 Ohm	5%

*** resistance results are fast and very accurate which minimizes iterations and gap between schematic and post layout simulation.**

*** Results on ST 28FDSOI**

CONCLUSION